AMENDMENTS TO SPECIFICATION

Page 1, lines 9-22:

Fig. 4 shows the structure of a single pixel in an active pixel sensor provided by the conventional metal oxide semiconductor manufacturing process, wherein the power of the pixel 41 is supplied by a power source VCC. In operating the pixel, a reset signal 'RESET' is first applied to resent the pixel 41. After an exposure time period, a row driving signal is applied so as to read a voltage value representing the photoelectric signal ~~form~~ from the output (Pixel Out) of the pixel. The readout voltage value is stored in a correlated double sampling (CDS) circuit 42. Subsequently, the pixel 41 is reset again and the reset voltage is stored in the correlated double sampling circuit 42. By subtracting the two readout voltages, a voltage difference ~~resulted~~ resulting from radiating the pixel 41 can be obtained, which can be used to eliminate the fixed pattern noise (FPN) caused by the critical voltage variance due to unmatched conditions in the transistor manufacturing process of the pixel 41.

Page 6, line 18 to Page 7, line 2:

A preferred circuit layout of the aforesaid circuit is illustrated in Fig. 2, wherein, two layers of overlapped metal wires 21 and 22 are used to connect to the voltage sources VRT1 and VRT2, so that the metal wires of the two different voltage sources are used to supply voltages to the photoelectric diode PD and other circuits. In addition to eliminating the interference of noise, there is saved some space of pixel layout. Fig. 3 shows a second preferred circuit layout, wherein two layers of ~~vertically~~ perpendicularly arranged metal wires 31 and 32 are used to connect to the voltage ~~source~~ sources VRT1 and VRT2, so as to further reduce the mutual interference caused by the parasitic capacitor of the metal wires.